REMARKS

Claims 1-18 are present for examination.

Drawings:

In paragraph 1 of the outstanding office action, the Examiner has indicated that Fig. 6 should be labeled as prior art. However, applicant does not believe that it is appropriate to label Fig. 6 as prior art. Fig. 6 shows the structure of a frame which is utilized by the present invention as well as the prior art. Thus, it appears inappropriate to label this figure as prior art.

Applicant is submitting herewith a substitute sheet for Fig. 5 which has an incorrect formula at the bottom of the drawing. The correct formula is (L-1) x N as stated in the written description as originally filed on page 3, line 8.

Changes to the Written Description

In paragraph 2 of the outstanding office action, the Examiner has indicated various portions of the specification which should be corrected. Applicant has carefully reviewed the specification and has made the changes requested by the Examiner as well as additional changes of a minor nature. No new matter has been added.

Claim Objections

In paragraph 4 of the outstanding office action, the Examiner has made objections to the claims. Applicant has reviewed the Examiner's comments and has made the appropriate changes. It is pointed out, that the Examiner has indicated that claims 1 and 18 are objected to. However, upon reviewing these claims, it seems that the Examiner intended to indicate that claims 1 and 17 are objected to. Further, in paragraph 6 of the office action, the Examiner refers to claim 18 but applicant believes the Examiner intended to refer to claim 17. The claims have been accordingly amended.

Prior Art Rejections under § 102

Claims 6, 9, 12 and 15 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Dabak (6,345,069).

The Examiner's rejection is respectfully traversed.

As to claim 6, the Examiner recognizes that "wherein the first data is supplied to the adder in a first period when the first data is written to the first memory" is disclosed in FIG. 8 and column 6, lines 48-53 of Suzuki. However, there is no disclosure in Dabak of the specific timing of operation of claim 6 which further recites: "wherein said second data and said first data which have been stored in said first memory are supplied to said adder in a second period when said second data are written to said second memory." In addition, "the shift register" which is referred to by the examiner in the rejection reason is not shown in the circuit as shown in FIG. 8 of Suzuki.

The Examiner recognized that "wherein the second data and the first data which have been stored in the first memory are supplied to the adder in a second period when the second data is written to the second memory" is disclosed in FIG. 8 and column 6, lines 48-53. However, there is no disclosure in Dabak of the specific timing of operation of claim 6. In addition, "a shift register" which is cited in the rejection reason is not shown in the circuit as shown in FIG. 8 of Dabak.

In view of the comments set forth above, it is submitted that the Dabak reference does not anticipate applicant's invention and that the section 102 rejection should be withdrawn.

Prior Art Rejections under § 103

Claims 1-5, 7, 8, 10, 11, 13, 14 and 16-18 stand rejected under 35 U.S.C. § 103 as unpatentable over Suzuki (5,903,595) in view of Dabak.

The Examiner's rejection is respectfully traversed.

As to claim 1, the Examiner asserts that "the spread code being of L x M period per symbol" corresponds the description in column 2, lines 2-8 of Suzuki. However, because the

length of "the spread code being of L x M period per symbol" is one symbol, whereas there is described in Suzuki that a long spread code has a length sufficiently longer than that of one symbol and the short spread code has substantially the same length as that of one symbol (column 2, lines 2-8 of Suzuki). That is, "L" does not correspond to the long spread code and "M" does not correspond to the short spread code. The apparatus of claim 1 concerns a signal spread by the spread code of L x M period per symbol, whereas the apparatus of Suzuki is not concerned with such a signal. Therefore, the apparatus of Suzuki has no relation to the apparatus of claim 1.

The Examiner asserts that "the M memories" corresponds to "the storage circuit 6" of Suzuki. However, this assertion is incorrect for the reasons as follows: (1) "each of the M memories" stores L x N samples of an intermediate correlation signals and L x N samples are a part of one symbol, whereas "the storage circuit 6" of Suzuki stores m symbols, (2) there are "the M memories" in claim 1, whereas there is only "the single memory 6" in Suzuki.

The Examiner further asserts the "the adder" corresponds to "the adding circuit 10" of Suzuki. However, this assertion is incorrect, because "the adder" inputs from each of the input terminals one of intermediate correlation signal which is outputted from the L-cbip accumulator and the intermediate correlation signal which is outputted from a corresponding memory; whereas "the adding circuit 10" if Suzuki always inputs from each of the input terminals a signal from the multiplier and does not select an input signal.

The Examiner also asserts that "the controller" corresponds to "the address signal generating circuit 11" of Suzuki. However, this assertion is incorrect for the reasons as follows: (1) "the controller" supplies the intermediate correlation signal to the M memories and the M input terminals of the adder in rotation with a unit of L x N samples, whereas "the address signal generating circuit 11" of Suzuki merely generates the address of the single storage circuit 6, does not supply the signals to any input terminal of the adder 10, and does not supply data to the storage circuit 6 in rotation with a unit of L x N samples, (2) "the controller" reads, and supplies to each of the input terminals of the adder, the intermediate correlation signal which has been stored in each of the memories M-1 times, whereas the data in the storage circuit 6 of Suzuki is read only once. The controller's repetitive operation of

M-1 times exploits the characteristics of the spread code of L x M in which the same sequence of length of L is repeated by M times with the same or opposite polarity, and is not similar to the operation of Suzuki which does not treat the spread code of L x M.

Regarding claim 7, the Examiner asserts that "the controller" corresponds to "the address signal generating circuit 11" of Suzuki. However, this assertion is incorrect because the operation of the controller is specifically defined as supplying the first correlation signals which have been stored in memories other than a first memory among the plurality of memories when the first correlation signal is written to the first memory, whereas such a specific operation is not disclosed in Suzuki,

Regarding claim 17, the Examiner asserts that "writing samples of the intermediate correlation signal to M memories in rotation with a unit of LX N samples" corresponds to "the address signal generating circuit 11" of Suzuki. However, the Examiner's assertion is incorrect because "the address signal generating circuit 11" does not write a signal to M memories in rotation with a unit of L X N samples.

The Examiner asserts that "supplying the samples of the intermediate correlation signal to M input terminals of an adder simultaneously with the step of writing" corresponds to the description in column 6, lines 7-10 of Suzuki. However, the Examiner's assertion is incorrect because the description in column (3, lines 7-10 of Suzuki does not relate to an adder.

The Examiner further asserts that "reading samples as many as LXN of said intermediate correlation signal which have been stored in each of said memories M-1 times" corresponds to the description in column 6, lines 7-10 of Suzuki. However, the Examiner's assertion is incorrect because reading a signal a number of times is not described in column 6, lines 7-10 of Suzuki.

In view of the comments set forth above, it is submitted that the rejection applying Suzuki even in view of Dabak cannot stand and that the section 103 rejection should be withdrawn. In short, the Patent and Trademark Office has not made out a prima facie case of obviousness under the provisions of 35 U.S.C. § 103.

Conclusion

The application is now believed to be in condition for allowance and an early indication of same is earnestly solicited.

Respectfully submitted,

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By _____

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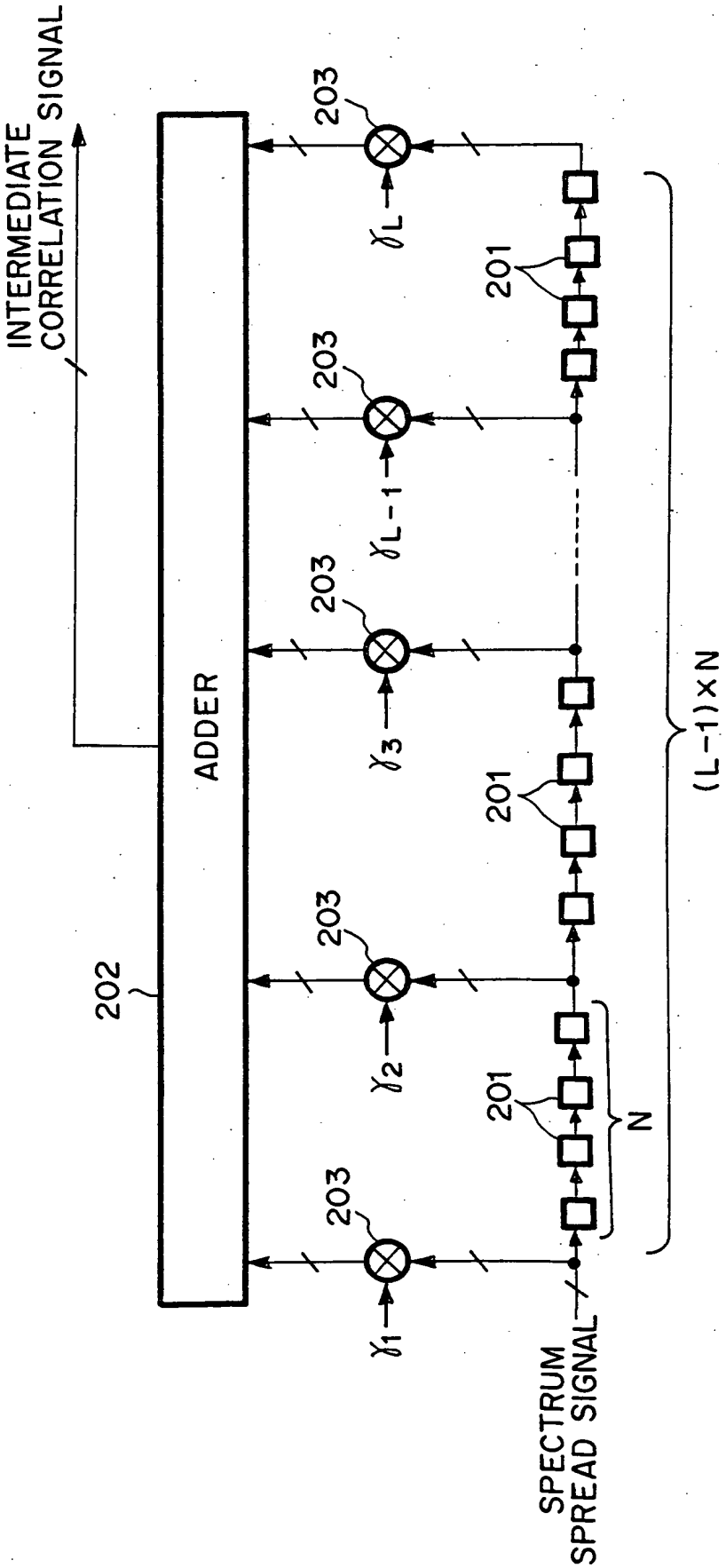
FIG.5


INTERMEDIATE CORRELATION SIGNAL
ADDER
202
203
201
γ_1
γ_2
γ_3
γ_{L-1}
γ_L
N
(L-1)×N
SPECTRUM SPREAD SIGNAL